pending claims have been canceled in favor of new claims 28-34. Because of substantial revisions, it was deemed best to submit a new set of claims.

The Drawing

The drawing is objected to for omitting reference number 22. In reviewing the application, a reference to the overall resistor device (the intention of reference number 22) is believed surperfluous, and confusing, which may be the reason it was left out. Every figure shows the overall resistor device, and nothing else. There is a reference to the resistor body (38), which is believed to be more suited to the organization of the description of the figures. For this reason, the specification has been amended to remove reference to the overall resistor.

Rejection on informalities

Paragraph 2. of the Office action refers to certain passages in the claims as either in error, or unclear. These have been eliminated in the new claims, especially in new claim 28, which is believed to make the intended structure clear.

Background Explanation

Prior to addressing the rejections of record, some of the salient features of applicants' invention will be reviewed.

The most consequential feature in the context of the prosecution to date is the single polysilicon contact that makes electrical contact to both the polysilicon field plate and to the resistor at the same time. It will be evident from viewing the

figures that this expedient saves chip area. The chip locations normally reserved for contact to the resistor reside to the sides of the field plate. For example, in a normal structure (see Figure 19) both of the resistor contacts lie outside the profile of the field plate. Moving one of the resistor contacts to the area BENEATH the field plate is made possible only by the window 44 in Fig. 4. That allows the contact 82 (Fig. 16) to simultaneously contact field plate 48' and the substrate resistor body 38. Therefore, in analyzing the prior art it is instructive to focus on the presence or absence of a window in the oxide that is formed between the field plate 48' and the resistor body 38. It is also pertinent, that in order to realize this structure in the manner claimed, one of the contacts to the resistor body is buried beneath the field plate.

The new claims are formulated to ensure that the contact from the field plate to the underlying resistor, i.e. one of the two resistor body contacts, is buried beneath the field plate. This feature is found in the following limitation of new claim 28:

> "a field plate on the first insulating layer, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,"

Since the polysilicon layer substantially covers the first insulating layer, and the first insulating layer is over the resistor body, and the polysilicon layer also fills the window in the first insulating layer and contacts the resistor, that should clearly convey the relationship that the window, and the resistor contact, necessarily lie

beneath the polysilicon field plate.

The Rejections On Prior Art

Turning to the rejections based on prior art, all claims previously pending were rejected under 35 U.S.C. 102 (b) as unpatentable over the Kondo patent.

With reference to Figs. 8 and 9 of the Kondo patent, which evidently are the most relevant, and those referred to by the Examiner, it can be seen that there are three distinct contacts provided for the resistor device, one for the field plate, and two for resistor body 35. They are designated 43-1, 43-2 and 43-3. By contrast, there are only two physical contacts for the resistor body 38 in applicants' device. These show in applicants' Fig. 14 as the contact that is formed in window 70, that contacts the resistor body 38 directly, and the contact that is formed in window 68, that contacts both the field plate 50, AND the resistor body 38 THROUGH the field plate 50. This can be compared with the Kondo device, but wherein the contacts 43-2 and 43-1 are made as a single contact. The saving in area in so doing is evident. But there is no teaching in Kondo, explicit or implied, of doing that.

Having established, it is hoped, a clear difference in the structure of applicant's device as compared with that of the reference, it remains to be sure that this difference is clearly set forth in the claims. To date, it appears that this may be the problem, i.e. that the wording of the claim, intended as defining applicant's novel structure, accidentally reads on the structure of the Kondo patent. However, in the new set of claims, it is believed that claim 28 clearly sets

forth a relationship wherein one of the resistor contacts is buried beneath the field plate, thus saving chip area.

An examination of the Kondo patent reveals that the insulating layer that separates the field plate and the resistor body has no window beneath the field plate. The field plate in Figs. 8 and 9 is element 39-1. There is no window in the insulating layer beneath element 39-1, and there is no portion of element 39-1 that extends through a window to the resistor body 35. Since there are no contacts underneath the field plate, all contacts to the substrate resistor body must lie outside the area of the polysilicon field plate, thus – in comparison with the arrangement of the invention – consuming unnecessary chip area.

At this point it should be evident that the invention, i.e. the problem and solution, are not mentioned or in any way anticipated by the Kondo patent.

The claims formerly pending also stand rejected as unpatentable over Japanese patent '723, in view of the Tamagawa patent. It is believed that, to the extent this rejection was applicable to the claims previously pending, that was due to the fact mentioned above, i.e. the claims did not specifically require that the contact between the field plate and the resistor body resides BENEATH the field plate, thus saving chip area. An examination of the Japanese patent reveals that the insulating layer 4' that separates the field plate and the resistor body has no window beneath the field plate. Moreover, there is no portion of field plate 20 that extends through a window in layer 4' to the resistor body 2. It is clear from the figures, note especially Fig. 8, that both of the contacts to the resistor body lie outside the profile of field plate 20, and neither is buried beneath the field plate as

required by applicant's new claims.

Nothing that appears in the Tamagawa patent would appear to provide the missing elements in the primary reference. The insulating layer in the Tamagawa patent has no windows, and there is no direct connection between a part of the field plate, through the intermediate insulating layer, to a resistor body.

The dependent claims, claims 29-34, rely largely on the features of claim 28 for patentability.

In view of the amendments and these remarks, reconsideration and allowance of claims 28-34 is requested.

In the event that the Examiner concludes that a telephone call would advance the prosecution of this application, the Examiner is invited and encouraged to call the undersigned attorney at Area Code 757-258-9018.

Respectfully,

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MARKED-UP SPECIFICATION

Four paragraphs beginning p. 4, line 4:

Figures 1-16 are a sequence of sectional views through a wafer or semiconductor substrate 20 illustrating steps in the method of fabricating a field plated resistor [22] with area thereover for routing metal conductors formed in the same layer of metal as contacts to the resistor are formed. The semiconductor substrate in a preferred embodiment is silicon, but the invention is not limited thereto. Other known semiconductor substrates may be used. While fabrication of a p-type silicon resistor is illustrated, the invention is not limited thereto. Although the method disclosed herein illustrates fabrication of a field plated resistor fabricated in the semiconductor substrate with metal contacts fabricated in the first layer of metal, the invention can be used to fabricate field plated resistors with metal contacts fabricated in higher layers of metal.

As shown in Figure 1, a tub or active area in which the field plated resistor [22] will be fabricated is developed in semiconductor substrate 20. An n+ implant step over the active area 24, followed by growth of an epitaxial layer of silicon approximately one micron thick, such as by a chemical vapor deposition process, results in a buried n+ layer 28 beneath the resulting upper surface 30 of substrate 20. The size and shape of active area 24 is dependent on the size of the field plated resistor(s) to be fabricated therein as well as the number of devices including field plated resistors contained therein.

The blanket etch step removes oxide (not shown) from upper surface 30 of substrate 20 to provide access to active area 24. Recesses 26, 32, and 34 are etched into the upper surface 30 of substrate 20 such as by a plasma etch process. An n+ implant into the deep collector is made top form contact 36 within the active area 24 but outside the resistor [22]. Contact 36 provides electrical access to the buried n layer 28 from upper surface 30. Field oxide is grown in the trenches for isolation, by any known process such as a recessed polybuffered LOCOS process. Simultaneous with growing the oxide, the n+ implant is diffused.

As illustrated in Figure 2, a mask of photoresist (not shown) is patterned over those portions of surface 30 where an implant is not desired. Portions of the active area 24 are implanted with a p+ dopant, such as but not limited to boron, to form resistor body 38. The amount of p-dopant implanted is determined by the resistance [resistor 22 is] desired [to have], as is known in the art. The photoresist is then removed.

Paragraph beginning at line 1, page 6:

Figure 5 is a cross sectional view of substrate 20 following a blanket deposition of a layer 48 of polysilicon, typically 3100 angstroms thick, over the amorphous polycrystalline silicon layer 42 by a chemical vapor deposition process. In addition to forming a layer over the amorphous polycrystalline silicon, the layer 48 of polysilicon fills window 44 making contact with resistor body 38 and defining a first resistor

contact 46. As part of a doped emitter process, layer 48 of polysilicon is implanted as shown in Figure 6 with a p-type dopant, such as but not limited to boron, to form a p-doped polysilicon. Doping the polysilicon could be achieved by other known methods. The implanting step is not required by the invention, but contributes to the field plated resistor [22] being fabricated in an existing process without adding additional processing steps. The p-type dopant forms an enhanced contact region 46' in contact 46. Enhanced contact region 46' is of lower resistance than contact 46.

Paragraph beginning at line 1 of page 7:

Another step not required by the invention but present in the existing process forms spacer 52 around the periphery of the polysilicon structures of emitter contacts (not shown) and field plate 50 formed from polysilicon layer 48 or 48'. A layer of insulative material such as TEOS oxide is deposited over the entire substrate 20. A dry etch process removes the unwanted insulative material, leaving spacer 52, as shown in Figure 8, around the periphery of polysilicon structures. Spacer 52 is typically 1500 angstroms in width at surface 30. In the existing process, spacer 52 is placed around the periphery of polysilicon structures to accommodate metal oxide semiconductove devices or self aligned devices fabricated on the same substrate. Spacer 52 self-aligns the second resistor contact 58 and allows greater utilization of the area over

the resistor body 38. While not necessary for the invention, this step contributes to fabricating field plated resistors [22] in an existing process without changing or adding process steps.

Paragraph beginning at line 16, page 8:

As illustrated in Figure 13, a first barrier layer 74, such as but not limited to platinum silicide, may be formed in each of windows 68, 70, and 72. Platinum is deposited over the substrate and heated to react with silicon where in contact therewith. Unreacted platinum is etched away, as is known in the art. First barrier 74 in window 68 is formed in field plate 50. First barrier layer 74 in window 70 is formed in the doped silicon in region 56 forming a second contact [76] to resistor body 38 [22]. First barrier layer 74 in window 72 is formed in the n+ doped silicon of contact 36.

Three paragraphs beginning at line 10, page 9:

Unwanted metal in layer 80 is etched away as known in the art, resulting in the field plated resistor [22] having traces extending thereover illustrated in Figures 16 and 17. Metal layer 80 provides a lead 82 to emitters (not shown) and field plate 50, a lead 84 to second resistor contact 58, a lead 86 to contact 36, and traces 88 of which traces 90 that are routed over resistor body 38 are a subset. [Field] The field plated resistor [22] illustrated in Figure 15 represents a portion of an integrated

circuit [98] in which the resistor [22] is fabricated. Thus, the field plated resistor [22] having an enhanced area over the body 38 of the resistor [22] is available for routing other metal conductors over body 38 [of resistor 22] in the same layer of metal as forms the contacts to the resistor.

Figure 17 is a top view of the field plated resistor [22] of Figure 16 showing one possible routing of conductors 90 over resistor body 38. The width 92 of the resistor body 38 is illustrated as being narrower in width than the width 94 of the first resistor contact 46 and second resistor contact 58 at ends of resistor body 38, although the invention is not limited thereto. Substantially all of the area over the resistor body 38 is available for routing traces or metal conductors, subject only to layout, design, and fabrication rules.

A field plated resistor [22] fabricated in this manner has an enhanced area over the resistor body 38 for routing conductors or traces 90. Layout, design, and fabrication rules may be limiting factors in [the] utilizing the area over resistor body 38 for routing conductors.